CHANNEL BONDING CONTROL LOGIC ARCHITECTURE

FIELD OF THE INVENTION

[0001] The present invention relates to data communication, and more specifically to a design for controlling multiple transceivers.

BACKGROUND OF THE INVENTION

[0002] As a result of improvement in processing technology, it is now possible to put millions of transistors in an integrated circuit. This increases the amount of processing power of the integrated circuit. However, the processing power may be wasted if there are insufficient input-output (I/O) resources to transfer data to and from the integrated circuit. High speed I/O transceivers alleviate this problem by increasing the data transfer speed of the I/O resources.

[0003] One way to increase the speed of I/O is to build better circuits (e.g., phase detector, charge pumps, filters, oscillators, etc.). Another way is to use multiple transceivers working in parallel. For example, data words in a transmitter can be split into bytes, with each byte sent over a separate transceiver. The bytes are received in parallel by separate transceivers in a receiver. The received bytes are then combined in the correct sequence to recover the original words. In the present invention, the communication path of each transceiver pair (one in the transmitter and one in the receiver) is called a "channel".

[0004] One of the problems of communication using parallel channels is that the data words may not be aligned properly when they reach the receiver. Fig. 1 is a drawing showing such as a situation. It shows four parallel buffers 112a-115a of a transmitter 102. Each buffer handles one byte of a four-byte word. For example, in order to transmit a full word contains bytes "SSSS", the first "S" is handled by the first

buffer, the second "S" is handled by the second buffer, etc. The arrows on top of the buffers indicate a transmission clock. Fig. 1 also shows the buffers of a receiver 104 that does not perform alignment. The arrows on top of the buffers indicate the sampling clock. It shows that the second buffer, 113b, is not aligned with the other buffers. One of the causes of the misalignment is variations in transmission delay, especially if the data streams are routed through repeaters. In this case, the received word will have the form "STSS", which is not the same as the transmitted word. Fig. 1 also shows the buffers of a receiver 106 that is able to perform alignment. It shows that the sampling clock is able to properly associate with the correct data, and the correct word can be recovered. This alignment process is also called "channel bonding."

[0005] One way to support correction of misalignment is to include in the data stream special byte sequences that define corresponding points in the several buffers. As illustration, it is assumed in Fig. 1 that the "P" bytes are special characters for this purpose. Each receiving transceiver recognizes the "P" character and remembers its location in the buffer. One transceiver will be designated as the master that instructs all the slave transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character). After this operation, the words will be properly aligned: RRRR, SSSS, TTTT, etc.

[0006] A transceiver may also perform other operations, such as clock correction. These collective operations are commonly called "elastic buffer" operations.

[0007] It can be seen from above that channel bonding is an important tool for increasing the speed of a communication system. Consequently, it is desirable to improve the operation of channel bonding.

SUMMARY OF THE INVENTION

[0008] The present invention involves a system for coordinating channel bonding operations of a plurality of transceivers. It comprises a master transceiver and a plurality of first level transceivers that perform channel bonding operations. Each first level transceiver is controlled by the master transceiver. The system also comprises a plurality of second level transceivers that perform channel bonding operations. Each second level transceiver is controlled by one of the plurality of first level transceivers.

[0009] One way to achieve the above coordination is to include a controller in the transceivers. This controller generates a first output control signal in response to a first and a second input signals. This output signal is used to control channel bonding operations. It comprises a first flip-flop that accepts the first input signal (the "master" signal) and generate an output signal. It also comprises a first multiplexer that has an output terminal and at least a first and a second input terminal. The first input terminal accepts the output signal of the first flip-flop, and the second input terminal is connected to the second input signal (the "channel bonding" input signal). The controller contains a second flip-flop that has an output terminal and an input terminal. The input terminal of the second flip-flop is connected to the output terminal of the first multiplexer. A second multiplexer having an output terminal and at least a first and a second input terminal is included in the controller. The first input terminal of the second multiplexer is connected to the output terminal of the second flip-flop, and the second input terminal is connected to the second input signal. The controller comprises a third flip-flop that has an output terminal to deliver the first output control signal. The input terminal of the third flip-flop is connected to the output terminal of the second multiplexer. A

mode signal is used to select one of the two input terminals of the two multiplexers.

[0010] In a further embodiment of the controller, it delivers a second output control signal (the "channel bonding" output signal). In this embodiment, the controller contains a third multiplexer that has at least a first and a second input terminals. The first input terminal is connected to the first input signal. The second input terminal is connected to the second input signal. The output terminal is connected to the input of a fourth flip-flop. The output of the fourth flip-flop delivers the second output control signal.

[0011] The above summary of the invention is not intended to describe each disclosed embodiment of the present invention. The figures and detailed description that follow provide additional exemplary embodiments and aspects of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a diagram showing the operation of channel bonding.

[0013] Fig. 2 is a diagram of a communication system of the present invention.

[0014] Fig. 3 is a block diagram of the input-output interface of a controller of the present invention.

[0015] Fig. 4 is a schematic diagram showing the connection of a plurality of transceivers of the present invention.

[0016] Fig. 5 is a block diagram of a portion of a controller of a transceiver of the present invention.

[0017] Fig. 6 is a diagram showing the equivalent circuit of a master transceiver and two slave transceivers.

DETAILED DESCRIPTION OF THE INVENTION

[0018] A communication system 130 of the present invention is shown in Fig. 2. It contains a first device 132 having a plurality of transceivers 134a-134d. One of the transceivers, such as transceiver 134a, is designated as the master. System 130 also contains a second device 136 having a plurality of transceivers 138a-138d. One of the transceivers, such as transceiver 138a, is designated as the master. Each transceiver in first device 132 is connected to the corresponding transceiver in second device 136 to form a channel. It should be noted that the master transceivers in the first and the second devices are not necessarily connected to one another.

[0019] When multiple transceivers operate in parallel as described above, the master transceiver controls channel bonding and clock correction operations in the slaves via control signal(s) connecting the several transceivers. One aspect of the invention is a method for the distribution of these control signals. The method allows an arbitrary group of transceivers to be channel bonded, provided the control signal routing between transceivers meets timing constraints.

[0020] Fig. 3 is a block diagram showing the input-output interface of a control section 150 of a transceiver of the present invention. Control section 150 contains the following input ports:

(a) a port 154 for accepting a control signal BON-M generated when this transceiver is designated a master;

(b) a port 156 for receiving a control signal BON-I from another transceiver when this transceiver is designated a slave; and

(c) a port 158 for receiving a clock signal CLK that is used to drive all the flip-flops in control section 150 (see Fig. 5 for more details).

[0021] The signal BON-M is preferably generated internally by the transceiver and delivered to control section 150.

[0022] Control section 150 also contains the following output ports:

(a) a port 160 for delivering a control signal BON-O to another transceiver; and

(b) a port 162 for delivering a control signal BON-C to the current transceiver for performing elastic buffer operations.

[0023] Control section 150 also contains a port 164 to accept a signal MODE. This signal identifies the mode of operation of the transceivers and is used to set the multiplexers in control section 150 (see Fig. 5 for details). In one embodiment, the modes are:

(a) OFF: The transceiver is not channel bonded with other transceivers.

(b) MASTER: The transceiver is a master.

(c) S_1_HOP: The transceiver is a slave that is controlled by a master transceiver.

(d) S_2_HOPS: The transceiver is a slave that is controlled by a S_1_HOP transceiver.

[0024] Fig. 4 is a schematic diagram showing the connection of different transceivers in accordance with the present invention. It shows a master transceiver 182 controlling a plurality of slave transceivers 184a and 184b. The BON-O control signal of the output port of master transceiver 182 is connected to the BON-I input port of the slave transceivers. Each slave transceiver controls a plurality of second level slave transceivers. For example, slave transceiver 184a controls transceivers 186a and 186b, while slave transceiver 184b controls transceivers 186c and 186d. The BON-O control signal of the output port of each slave transceivers is connected to the BON-I input port of the corresponding second level slave transceivers.

[0025] It should be noted that more levels of slave transceivers can be handled using the principle of the present invention.

[0026] Fig. 5 is a block diagram of a portion 200 of the control section of a transceiver of the present invention.

This portion accepts the input signals BON-I and BON-M, and then generates the output signals BON-C and BON-O. Portion 200 contains three multiplexers 202-204 and four flip-flops 206-209. The flip-flops are clocked by the same clock signal CLK received by the control section. The multiplexers are controlled by the same MODE signal received by the control section. Each multiplexer selects one of two input signals as output. The selection is determined by the MODE signal. For example, when the MODE signal is set at S_1_HOP or S_2_HOPS, the first input terminal of multiplexer 202 is selected while when MODE signal is set at MASTER, the second input terminal of multiplexer 202 is selected. It should be noted that Fig. 5 only shows a design that is used to process one bit of a multi-bit signal. Thus, portion 200 needs to be duplicated for a multi-bit system. For example, if the control and output signals are four-bit wide, each transceiver should have four copies of portion 200.

[0027] One characteristic of the present invention is that the number of flip-flop stages from the master's BON-M signal to any transceiver's BON-C signal (in the master and first and second level slaves) is the same. In this embodiment, the number of flip-flops is three. This will be illustrated in Fig. 6. This arrangement ensures that elastic buffer operations specified by the master will occur simultaneously in all the bonded transceivers.

[0028] Fig. 6 is a diagram showing the equivalent circuit of three transceivers: one master 232, one first level slave 234, and one second level slave 236. In master transceiver 232, there are three flip-flops 242-244 between signal BON-M to signal BON-C and one flip-flop 246 between signal BON-M and BON-O. Referring to Fig. 5, this is the situation where the MODE signal selects the bottom inputs of the multiplexers 202-204.

[0029] In the first level slave transceiver 234, there are two flip-flops 252-253 between signal BON-I and signal BON-C. Referring to Fig. 5, this is the situation where the MODE

signal selects the middle inputs of multiplexers 202-204. Together with flip-flop 246, there are three flip-flops from signal BON-M to BON-C of transceiver 234.

[0030] In the second level slave transceivers 236, there is one flip-flop 262 between signal BON-I and signal BON-C. Referring to Fig. 5, this is the situation where the MODE signal selects the top inputs of multiplexers 202-204. Together with flip-flops 246 and 256, there are three flip-flops from signal BON-M to BON-C of transceiver 236.

[0031] One advantage of the present invention is that the channel bonding control signals are not required to propagate from the master to all the slaves in a single clock cycle. The control signals need propagate only to the first level slaves in one clock cycle, and then use an additional clock cycle to propagate thence to the second level slaves. This increases the permissible control signal propagation delay between the master and the most remotely located slave transceivers. The invention also incurs minimal propagation delay for BON-I and BON-O inside the transceiver: BON-O comes directly from a flip-flop, and BON-I has only a single multiplexer delay before reaching any flip-flop. This further increases the propagation delay that may be allocated to control signal routing between the transceivers.

[0032] Another advantage of the present invention is that any transceiver may be designated as a master or a slave by the setting of the MODE signals. For a given collection of transceivers, any subset could be channel bonded by appropriate setting of the MODE signals and corresponding interconnection of BON-O and BON-I control signals for the transceivers in the subset. It is even possible to create multiple, disjoint subsets of channel-bonded transceivers within the given collection.

[0033] These advantages are particularly attractive for transceivers associated with a field-programmable gate array ("FPGA"). In this environment, transceivers may be widely separated, so that propagation delay of channel bonding

control signals between transceivers is a significant problem. Also, the FPGA's programmable routing resources may be used for the channel bonding control signals, facilitating the creation of arbitrarily defined subsets of transceivers that are channel bonded. This capability is desirable in FPGAs, which are intended to be easily configurable for a broad variety of applications.

[0034] These advantages may be attractive in other environments as well, for example, for channel bonding transceivers across multiple integrated circuit chips.

[0035] In order to properly carry out the operation of the present invention, the elastic buffer control signals (BON-C) are preferably computed three clock cycles before they are used. This implies that the master's elastic buffer control logic, including any necessary FIFO address generation, is operating in a "lookahead" fashion to generate BON-M in a timely way.

[0036] Those having skill in the relevant arts of the invention will now perceive various modifications and additions which may be made as a result of the disclosure herein. Accordingly, all such modifications and additions are deemed to be within the scope of the invention, which is to be limited only by the appended claims and their equivalents.